Amendments to the Claims:

Please amend claims 1, 5, 6, 7, 11, and 12 as follows.

This listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of claims:

1. (currently amended) An input buffer, comprising:

a single pull-up transistor connected between a power supply voltage and an input pad and having a gate to which a control voltage is applied, and having a substrate to which a floating well voltage is applied;

a transmission transistor having a gate to which the power supply voltage is applied and a substrate connected to a ground voltage, and transmitting at an output terminal a signal applied to the input pad;

a buffer having an input terminal coupled directly and exclusively to the output terminal of the transmission transistor, the buffer generating an input signal by buffering the signal transmitted by the transmission transistor; and

a controller generating the voltage of the signal applied to the input pad as the control voltage and the floating well voltage when a high voltage is applied to the input pad, and generating the ground voltage as the control voltage ~~in the case where a voltage less than the high voltage is applied to the input pad,~~ and ~~generating~~ the power supply voltage as the floating well voltage in the case where a voltage less than the high voltage is applied to the input pad.

2. (original) The input buffer of claim 1, wherein the high voltage is greater than the power supply voltage.

3. (original) The input buffer of claim 1, wherein the controller comprises:

a high voltage detecting circuit generating a high voltage detecting signal when the high voltage is applied to the input pad;

a high voltage detecting reset circuit generating a high voltage detecting reset

signal for resetting the high voltage detecting signal, when the voltage less than the high voltage is applied to the input pad; and

a control voltage and floating well voltage generating circuit generating the voltage applied to the input pad as the control voltage and the floating well voltage when the high voltage detecting signal is generated, and generating the ground voltage as the control voltage and the power supply voltage as the floating well voltage when the high voltage detecting signal is reset.

4. (original) The input buffer of claim 3, wherein the high voltage detecting circuit comprises:

a first PMOS transistor connected between the input pad and a first node and having a gate to which the power supply voltage is applied, and having a substrate to which the floating well voltage is applied;

a first NMOS transistor connected between the first node and a second node and having a gate to which the power supply voltage is applied, and having a substrate to which the ground voltage is applied;

a second NMOS transistor having a drain connected to the second node, a gate to which the high voltage detecting reset signal is applied, and a source and a substrate connected to the ground voltage;

a second PMOS transistor having a source and a substrate connected to the power supply voltage, and a gate connected to the first node;

a third PMOS transistor having a source connected to a drain of the second PMOS transistor, a gate connected to the second node, and a substrate connected to the power supply voltage; and

a third NMOS transistor having a gate connected to the second node, a drain connected to a drain of the third PMOS transistor, and a source and a substrate connected to the ground voltage; and

wherein the high voltage detecting signal is generated at the drain of the third PMOS transistor.

5. (currently amended) The input buffer of claim 3, wherein the high voltage detecting reset circuit comprises:

a first ~~fourth~~ NMOS transistor connected between the input pad and a ~~third~~ first node and having a gate to which the power supply voltage is applied, and having a substrate connected to the ground voltage;

a first ~~fourth~~ PMOS transistor having a source and a substrate to which the power supply voltage is applied, and a gate connected to the input pad;

a second ~~fifth~~ PMOS transistor having a source connected to a drain of the first ~~fourth~~ PMOS transistor, a substrate to which the power supply voltage is applied, and a gate connected to the first ~~third~~ node; and

a second ~~fifth~~ NMOS transistor having a drain connected to a drain of the second ~~fifth~~ PMOS transistor, a gate connected to the first ~~third~~ node, and a source and a substrate connected to the ground voltage; and

wherein the high voltage detecting reset signal is generated at the drain of the fifth PMOS transistor.

6. (currently amended) The input buffer of claim 3, wherein the control voltage and floating well voltage generating circuit comprises:

a first ~~sixth~~ PMOS transistor having one of a source and drain to which the power supply voltage is applied, a gate connected to a first ~~fourth~~ node, and the other of the drain and source and a substrate to which the floating well voltage is applied;

a second ~~seventh~~ PMOS transistor having one of a source and drain connected to the first ~~fourth~~ node, a gate to which the power supply voltage is applied, the other of the drain and source connected to the input pad, and a substrate to which the floating well voltage is applied;

a third ~~an eighth~~ PMOS transistor having one of a source and drain and a substrate to which the floating well voltage is applied, the other of the source and drain connected to the input pad, and a gate to which the power supply voltage is applied ~~a gate connected between the fourth node and the input pad and to which the power supply voltage is applied, and having a substrate to which the floating well voltage is~~

~~applied~~;

a first ~~sixth~~ NMOS transistor having a gate to which the power supply voltage is applied, a drain connected to the first ~~fourth~~ node, and a substrate connected to the ground voltage; and

a second ~~seventh~~ NMOS transistor having a drain connected to a source of the first ~~sixth~~ NMOS transistor, a gate to which the high voltage detecting signal is applied, a substrate and a source connected to the ground voltage; and

wherein the control voltage is generated at the first ~~fourth~~ node and the floating well voltage is generated at the one of the drain and source of the first ~~sixth~~ PMOS transistor.

7. (currently amended) An input buffer, comprising:

a single pull-up transistor connected between a power supply voltage and an input pad;

a transmission transistor having a gate to which the power supply voltage is applied and a substrate connected to a ground voltage, and transmitting at an output terminal a signal applied to the input pad;

a buffer having an input terminal coupled directly and exclusively to the output terminal of the transmission transistor, the buffer generating an input signal by buffering the signal transmitted by the transmission transistor; and

a controller turning off the single pull-up transistor when a high voltage is applied to the input pad, and turning on the single pull-up transistor in the case where a voltage less than the high voltage is applied to the input pad.

8. (original) The input buffer of claim 7, wherein the controller comprises:

a high voltage detecting circuit generating a high voltage detecting signal when the high voltage is applied to the input pad, and resetting the high voltage detecting signal in the case where a voltage less than the high voltage is applied to the input pad; and

a control voltage and floating well voltage generating circuit applying a voltage

applied to the input pad to a gate and a substrate of the pull-up transistor when the high voltage detecting signal is generated, and applying the ground voltage and the power supply voltage to the gate and the substrate of the pull-up transistor in the case where the high voltage detecting signal is reset.

9. (original) The input buffer of claim 8, wherein the high voltage detecting circuit comprises:

a high voltage detecting circuit generating a high voltage detecting signal when a high voltage is applied to the input pad; and

a high voltage detecting reset circuit generating a high voltage detecting reset signal for resetting the high voltage detecting signal, in the case where a voltage less than the high voltage is applied to the input pad.

10. (original) The input buffer of claim 9, wherein the high voltage detecting circuit comprises:

a first PMOS transistor connected between the input pad and a first node and having a gate to which the power supply voltage is applied, and having a substrate to which the floating well voltage is applied;

a first NMOS transistor connected between the first node and a second node and having a gate to which the power supply voltage is applied, and having a substrate to which a ground voltage is applied;

a second NMOS transistor having a drain connected to the second node, a gate to which the high voltage detecting reset signal is applied, and a source and a substrate connected to the ground voltage;

a second PMOS transistor having a source and a substrate connected to the power supply voltage, and a gate connected to the first node;

a third PMOS transistor having a source connected to a drain of the second PMOS transistor, a gate connected to the second node, and a substrate connected to the power supply voltage; and

a third NMOS transistor having a gate connected to the second node, a drain

connected to a drain of the third PMOS transistor, and a source and a substrate connected to the ground voltage; and

wherein the high voltage detecting signal is generated at the drain of the third PMOS transistor.

11. (currently amended) The input buffer of claim 9, wherein the high voltage detecting reset circuit comprises:

a first ~~fourth~~ NMOS transistor connected between the input pad and a first ~~third~~ node and having a gate to which the power supply voltage is applied, and having a substrate connected to the ground voltage;

a first ~~fourth~~ PMOS transistor having a source and a substrate to which the power supply voltage is applied, and a gate connected to the input pad;

a second ~~fifth~~ PMOS transistor having a source connected to a drain of the first ~~fourth~~ PMOS transistor, a substrate to which the power supply voltage is applied, and a gate connected to the first ~~third~~ node; and

a second ~~fifth~~ NMOS transistor having a drain connected to a drain of the second ~~fifth~~ PMOS transistor, a gate connected to the first ~~third~~ node, and a source and a substrate connected to the ground voltage; and

wherein the high voltage detecting reset signal is generated at the drain of the fifth PMOS transistor.

12. (currently amended) The input buffer of claim 8, wherein the control voltage and floating well voltage generating circuit comprises:

a first ~~sixth~~ PMOS transistor having one of a source and drain to which the power supply voltage is applied, a gate connected to a first ~~fourth~~ node, the other of the drain and source to which the floating well voltage is applied, and a substrate;

a second ~~seventh~~ PMOS transistor having one of a source and drain connected to the first ~~fourth~~ node, a gate to which the power supply voltage is applied, the other of the drain and source connected to the input pad, and a substrate to which the floating well voltage is applied;

a third ~~an eighth~~ PMOS transistor having one of a source and drain and a substrate to which the floating well voltage is applied, the other of the source and drain connected to the input pad, and a gate to which the power supply voltage is applied ~~a gate connected between the fourth node and the input pad and to which the power supply voltage is applied, and a substrate to which the floating well voltage is applied~~;

a first ~~sixth~~ NMOS transistor having a gate to which the power supply voltage is applied, a drain connected to the first ~~fourth~~ node, and a substrate connected to the ground voltage; and

a second ~~seventh~~ NMOS transistor having a drain connected to a source of the first ~~sixth~~ NMOS transistor, a gate to which the high voltage detecting signal is applied, and a substrate and a source connected to the ground voltage; and

wherein the control voltage is generated through the first ~~fourth~~ node and the floating well voltage is generated through the drain or source of the first ~~sixth~~ PMOS transistor.